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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/595,508	06/14/2000	Lawrence Larson	UCSD 99-116	8936

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William C Fuess
Fuess & Davidenas
10951 Sorrento Valley Road
Suite II-G
San Diego, CA 92121-1613

EXAMINER	
RAMPURIA, SHARAD K	
ART UNIT	PAPER NUMBER
2683	

DATE MAILED: 01/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/595,508	LARSON ET AL.	
	Examiner	Art Unit	
	Sharad Rampuria	2683	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-10 & 16 are rejected under 35 U.S.C. 102 (a) as being anticipated by Wei Xiong and Lawrence E. Larson. (IEEE Radio Frequency Integrated Circuits Symposium, 1999)

1. Regarding claim 1, Wei Xiong and Lawrence E. Larson disclosed A method of operating an amplifier, which amplifier has an load line, (Fig.2)

to emulate the property of a class AB amplifier where increasing amplifier input current raises the d.c. bias of the amplifier and increases amplifier output current, (Second Paragraph; Page. 194)

nonetheless that the amplifier will never enter class AB operation and will always operate in class A, the method of operating an amplifier always in class A nonetheless to producing more output current from more input current comprising: (Third Paragraph; Page. 195)

monitoring the amplified output of the class A amplifier; and, in response to detecting an increase in the amplifier output, dynamically biasing the load line of the amplifier to a higher d. c . bias point, causing the amplifier to consume more power and to produce a still larger amplified output signal, nonetheless to maintaining operation of the amplifier always in class A. (Fourth Paragraph; Page. 195)

2. Regarding claim 2, Wei Xiong and Lawrence E. Larson disclosed The class A amplifier operating method according to claim 1 used on a class A amplifier serving as an initial low noise radio signal amplifier in a wireless communication system;

wherein an increase in amplifier output signal is indicative of a presence of a strong jammer component in the amplifier input signal, so that moving the load line of the amplifier will cause the amplifier to draw more current beneficially decreasing a noise figure while increasing gain of the amplifier, and causing the amplifier to reach a new steady state with higher power and improved linearity. (Third Paragraph; Page. 195)

Wherein when no increase in amplifier output signal is detected, indicative that no strong jammer component is present within the amplifier input signal, then neither the d.c. bias, nor the load line, will be raised, and the amplifier will operate quiescently, conserving power. (Fourth Paragraph; Page. 195)

3. Regarding claim 3, Wei Xiong and Lawrence E. Larson disclosed An amplifier comprising:

at least one Field Effect Transistor (FET) receiving at its gate an input signal from an external source and amplifying this input signal in accordance with its drain-source bias voltage VDs to produce at its drain an amplified output signal; (Third Paragraph; Page. 194)

a power detector circuit monitoring the amplified output signal to produce a detected-power voltage signal VDD; (Eq.1; Third Paragraph; Page. 194)

a dynamic bias control circuit comparing the detected-power signal VDD to the drain-source bias voltage VDS to vary a gate-to source voltage bias VS of the input signal, actively moving a load line of the FET so as to cause the FET to consume more power when the amplified output signal is large; (Eq.1; Third Paragraph; Page. 194)

wherein when the amplified output signal is large because of a presence of a strong jammer component of the input signal, then the moved load line of the at least one FET will cause the FET to draw more current decreasing noise figure while increasing gain, and will cause the amplifier of which the at least one FET forms a part to reach a new steady state with higher power and improved linearity; (Fourth Paragraph; Page. 194)

wherein, however, when no strong jammer component of the input signal is present, and when the amplified output signal is correspondingly not large, then the FET, and the amplifier of which it forms a part, will conserve power; wherein a self-adjusting bias of the at least one FET results in improved power consumption and improved dynamic range in an environment where exists occasional strong jammer signals. (Third Paragraph; Page. 195)

4. Regarding claim 4, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 3 wherein the at least one Field Effect Transistor (FET) comprises:

two cascaded FETs. (Abstract & Fig.3; Third Paragraph; Page. 194)

5. Regarding claim 5, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 4 wherein the each of the wo cascaded FETs comprises:

a GaAS FET. (Abstract & Fig.3; Third Paragraph; Page. 194)

6. Regarding claim 6, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 4 wherein a first, input, one of the two cascaded FETs comprises:

a low-noise PHEMT; (Fig.3; Third Paragraph; Page. 194)

and wherein a second, output, one of the two cascaded FETs comprises:

a hetero-junction FET. (Fig.3; Third Paragraph; Page. 194)

7. Regarding claim 7, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 3 wherein the dynamic bias control circuit comprises:

two operational amplifiers each varying a gate-to-source voltage bias VAS of an associated FET. (Fig.3; Third Paragraph; Page. 194)

8. Regarding claim 8, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 3 wherein the power detector circuit comprises:

a resistor R; (Fig.3) and

a first diode D1 series connected to form a diode-limited resistive divider. (Fig.3; Third Paragraph; Page. 194)

9. Regarding claim 9, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 8 wherein the diode-limited resistive divider and first diode D1 are both temperature compensated by a second diode D2. (Fig.3; Third Paragraph; Page. 194)

10. Regarding claim 10, Wei Xiong and Lawrence E. Larson disclosed The amplifier according to claim 3 wherein the power detector circuit is temperature compensated. (First Paragraph; Page. 195)

16. Regarding claim 16, Wei Xiong and Lawrence E. Larson disclosed A circuit for detecting a peak power of an a.c. signal, the peak power detector circuit comprising:
a resistive voltage divider, located between a voltage source and ground, producing a reference voltage signal;
(Fig.3; Third Paragraph; Page. 194)
a diode connecting at its cathode to both the a.c. signal and to the reference voltage signal;
(Fig.3; Third Paragraph; Page. 194)
an envelope detector connected both to the anode of the diode and to the reference voltage; (Fig.3; Third Paragraph; Page. 194)
wherein output of the detector circuit appears across the envelope detector; (Fig.3; Third Paragraph; Page. 194)
wherein when the a. c. signal is zero then the detector circuit output is equal to the reference voltage;
(Fig.3; Third Paragraph; Page. 194)
wherein when the a.c. signal is not zero then the detector circuit output is equal to a sum of (i) the reference voltage, and (ii) a voltage of an envelope of the a.c. signal, which voltage of the envelope of the a.c. signal is equivalent to the power of the a.c. signal. (Fig.3; Third Paragraph; Page. 194)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wei Xiong and Lawrence E. Larson in view of Fujita.

11. Regarding claim 11, Wei Xiong and Lawrence E. Larson ***does not disclose expressly,*** The amplifier operational in S band***, but they shows in the title of the paper*** "An S-band Low Noise Amplifier with Self-Adjusting Bias for Improved Power Consumption and Dynamic Range in a Mobile Environment", IEEE Radio Frequency Integrated Circuits Symposium, 1999, The amplifier ***(Fig.3) which would inherently contains*** The amplifier according to claim 3 operational in S band. Also it is known in the art that 2.4GHz falls in S band category.

Furthermore, Wei Xiong and Lawrence E. Larson disclosed all the particulars of the claim except the operation in S band. However, Fujita teaches in an analogous art, that The amplifier according to claim 3 operational in S band. (Col.6;

53-58) Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the operation in S band in order to minimize the cost and size of the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sharad Rampuria whose telephone number is 703-308-4736. The examiner can normally be reached on Mon-Thu.(6:30-4:00) alternate Fri.(6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 703-308-5318. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

WILLIAM TROST
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

SK
January 10, 2003